ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

Check for updates

Sub 10 nm Bilayer Bi_2O_2Se Transistors

Jie Yang, Ruge Quhe, Qiuhui Li, Shiqi Liu, Lianqiang Xu, Yuanyuan Pan, Han Zhang, Xiuying Zhang, Jingzhen Li, Jiahuan Yan, Bowen Shi, Hua Pang, Lin Xu, Zhiyong Zhang, Jing Lu,* and Jinbo Yang**

Due to high carrier mobility and excellent air stability, emerging 2D semiconducting Bi_2O_2Se is attracting much attention as a potential channel candidate for the next-generation field effect transistor (FETs). Although the fabricated bilayer (BL) and few layers Bi_2O_2Se FETs exhibit a large current on/off ratio (>10^6) and a near-ideal subthreshold swing value (≈65 mV dec^{-1}), the performance limit of ultrashort channel Bi_2O_2Se FET is obscure. Here the ballistic performance upper limit of the sub 10 nm BL Bi_2O_2Se metal-oxide-semiconductor FETs (MOSFETs) is simulated for the first time by using ab initio quantum transport simulations. The optimized BL Bi_2O_2Se n-type MOSFETs can fulfill the high performance device requirements on the on-state current, delay time, and power dissipation of the International Technology Roadmap for Semiconductors in 2028 until the gate length is scaled down to 5 nm. Therefore, Moore's law can be extended to 5 nm by taking BL Bi_2O_2Se as the channel.

1. Introduction

Field effect transistors (FETs) with a channel length smaller than 10 nm are the compelling demand for the electronics quest in the next decade.[1–4] However, Moore's law has approached its physical limit because silicon FETs scaling down to 10 nm gate length especially for the sub 5 nm node is difficult to have satisfactory performance caused by the severe short channel effect.[1,5,6] To extend Moore's law down to sub 10 nm, 2D semiconductors are proposed as the next-generation channel candidates to replace silicon.[2,7–10] Their atomic thickness benefits the improvement of gate electrostatic controlling ability, and their uniform and free-dangling-bond structures lead to improved transporting efficiency.[5,11–14] The most extensively concerned 2D semiconductors are transition metal dichalcogenides (TMDs) like 2D MoS_2 and black phosphorene (BP).[10,15–20] The 1 nm L_g bilayer (BL) MoS_2 FET and 8.2 nm L_g monolayer (ML)/9.6 nm L_g multilayer MoS_2 FETs are successfully fabricated.[1,3,21] However, 2D MoS_2 FETs with low carrier mobility (≈270 cm^2 V^{-1} s^{-1}),[22–26] suffer from low on-state current (≈20 μA $μm^{-1}$)[1] and thus poor device switching speed. BP FETs possess a high carrier mobility (≈1000 cm^2 V^{-1} s^{-1}) but are instable under ambient condition.[27–29] It is urgent to explore 2D semiconductors with high carrier mobility, air stability, and superior device performances in logic devices simultaneously.

Very recently, ML, BL, and few layers Bi_2O_2Se are successfully fabricated on mica substrate by means of chemical vapor deposition (CVD) method.[30–32] Bi_2O_2Se, as a typical bismuth-based oxychalcogenide semiconductor, is composed by Bi_2O_2 layers and Se layers under weak electrostatic interaction.[8,22,32–34] Remarkably, 2D Bi_2O_2Se has an ultrahigh electron mobility (>20 000 cm^2 V^{-1} s^{-1} at low temperature, ≈450 cm^2 V^{-1} s^{-1} at room temperature), which exceeds that of MoS_2.[30–32,35–37] 2D Bi_2O_2Se down to monolayer shows robust stability in air, and in moist or thermal conditions.[32] Since the stability is a precondition for large-scale production, 2D Bi_2O_2Se is a more feasible candidate of the next-generation channel material compared with BP. So far, the ML Bi_2O_2Se high performance devices have not been fabricated yet due to a big contact resistance while the long channel top-gated high performance BL and few layer Bi_2O_2Se FETs with Au/Pd electrode have been fabricated and exhibited a large current on/off ratio (>10^6).[32] However, the performance upper limit of BL Bi_2O_2Se FET in ultrashort channel remains unknown. Therefore, it is highly desirable to explore whether sub 10 nm BL Bi_2O_2Se FET can meet the

Dr. J. Yang, Dr. S. Liu, Prof. L. Xu, Dr. Y. Pan, Dr. H. Zhang, Dr. X. Zhang, Dr. J. Li, J. Yan, Dr. B. Shi, H. Pang, Prof. J. Lu, Prof. J. Yang
State Key Laboratory for Mesoscopic Physics and Department of Physics
Peking University
Beijing 100871, P. R. China
E-mail: jinglu@pku.edu.cn; jbyang@pku.edu.cn

Prof. R. Quhe, Q. Li, Prof. L. Xu
State Key Laboratory of Information Photonics
and Optical Communications and School of Science
Beijing University of Posts and Telecommunications
Beijing 100876, P. R. China
E-mail: quheruge@bupt.edu.cn

Prof. L. Xu
School of Physics and Electronic Information Engineering
Engineering Research Center of Nanostructure and Functional Materials
Ningxia Normal University
Guyuan, Ningxia 756000, P. R. China

Dr. L. Xu, Prof. Z. Zhang
Key Laboratory for the Physics and Chemistry of Nanodevices
and Department of Electronics
Peking University
Beijing 100871, P. R. China

Prof. J. Lu, Prof. J. Yang
Collaborative Innovation Center of Quantum Matter
Beijing 100871, P. R. China

Prof. J. Lu, Prof. J. Yang
Beijing Key Laboratory for Magnetoelectric Materials and Devices
Peking University
Beijing 100871, P. R. China

DOI: 10.1002/aelm.201800720

© 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

requirements of International Technology Roadmap for Semiconductors (ITRS)[38] in the next decade.

In this work, we theoretically evaluate the device performance of the sub 10 nm double-gated (DG) BL Bi_2O_2Se metal-oxide-semiconductor FETs (MOSFETs) using ab initio quantum transport simulations. The highest on-state current of the BL Bi_2O_2Se p-MOSFETs without underlap (UL) structure could only fulfill ≈55% high performance (HP) ITRS goals at L_g = 9 nm while it can increase to ≈77% HP on-state current requirement of the ITRS with help of underlap structure. The BL Bi_2O_2Se n-MOSFETs could not fulfill the HP ITRS goals without underlap structure while with the resort of underlap structure, they could meet the standard of on-state current, delay time, and power dissipation indicator (PDP) of ITRS goals for HP devices until L_g scaling down to 5 nm. Therefore, BL Bi_2O_2Se is a potential channel material for sub 10 nm transistor due to its high device performance and high stability.

2. Methodology

The transport properties are calculated by using the density functional theory (DFT) coupled with the nonequilibrium Green's function (NEGF) formalism, as implemented in the Atomistix ToolKit 2017 package.[39,40] The transmission coefficient $T_{k_{//}}(E)$ ($k_{//}$ stands for the reciprocal lattice vector along the surface-parallel direction in the irreducible Brillouin zone) is represented by[5,41]

$$T_{k_{//}}(E) = Tr\left[\Gamma^{l}_{k_{//}}(E) G_{k_{//}}(E) \Gamma^{r}_{k_{//}}(E) G^{\dagger}_{k_{//}}(E)\right] \quad (1)$$

where $G_k(E)$ and $G^{\dagger}_{k_{//}}(E)$ stand for the retard and advanced Green's function, respectively, and $\Gamma^{r}_{k_{//}}(E) = i\left(\Sigma_{l/r} - \Sigma^{\dagger}_{l/r}\right)$ is the broadening width originating from left/right electrode in the form of self-energy $\Sigma_{l/r}$. Given a certain energy, $T_{k_{//}}(E)$ is averaged over all different $k_{//}$. The drain current I_{ds} is calculated through the following Landauer–Bűttiker formula[42–44]

$$I_{ds}(V_b, V_g) = \frac{2e}{h} \int_{-\infty}^{+\infty} \left\{T(E, V_b, V_g)\left[f_S(E-\mu_S) - f_D(E-\mu_D)\right]\right\} dE \quad (2)$$

where f_S and f_D are the Fermi–Dirac distribution function for the source and drain, respectively, μ_S and μ_D are the Fermi level of the source and drain, respectively. The double zeta polarized basis set (DZP) is adopted. The temperature is set to 300 K, and the real-space mesh cutoff is taken as 75 hartree. The k-point meshes for the electrode region and the central region are 35 × 1 × 35 and 35 × 1 × 1, respectively. The generalized gradient approximation (GGA) in the form of Perdew–Burke–Ernzerhof (PBE) potential is employed to describe the exchange correlation interaction.[45] In the FET configuration, electron–electron interaction of the channel is heavily weakened by the introduced carriers. The DFT-GGA method based on single electron approximation approaches the quasiparticle method and is accurate enough to describe the electronic structure of this case.[46–48] For example, the bandgap of degenerately doped ML $MoSe_2$ is 1.52 eV at DFT-GGA level,[49] which is in great consistency with the value of 1.59 eV calculated by quasiparticle method within GW approximation[48] and 1.58 eV obtained by angle-resolved photoemission spectroscopic.[50] For another example, the calculated transport gap of ML, BL, and trilayer BP with Ni electrode at the DFT-GGA level is 0.65, 0.81, and 0.68 eV, in good accordance with the experimentally measured value of 1.00, 0.71, and 0.61 eV respectively.[51–53]

3. Results and Discussions

3.1. Model and Device

Unlike the well-known 2D materials, such as few layers MoS_2 and BP, which are stacked via interlayer van der Waals interaction, 2D Bi_2O_2Se is separated by charge-compensating cations and anions. Se^{2-} anionic layer is sandwiched by $(Bi_2O_2)^{2+}$ cationic layers via electrostatic interaction.[30] To balance the nonstoichiometry caused by additional Se layer in 2D Bi_2O_2Se, hydrogen atoms are added to passivate the outmost Se atoms.[35] The bulk Bi_2O_2Se has a tetragonal structure with lattice constants of $a = b = 3.88$ Å and $c = 12.16$ Å.[32] The optimized lattice parameters of BL Bi_2O_2Se is $a = b = 3.98$ Å (**Figure 1**a). The calculated bandgap of BL Bi_2O_2Se is 0.18 eV at the DFT-GGA level (Figure 1b), which is in agreement with the previously calculated value at the DFT-GGA level.[32] The two-probe DG BL Bi_2O_2Se MOSFET is constructed with intrinsic BL Bi_2O_2Se as channel and n-doped or p-doped BL Bi_2O_2Se as electrode in semi-infinite length, as shown in **Figure 2**a. The segments

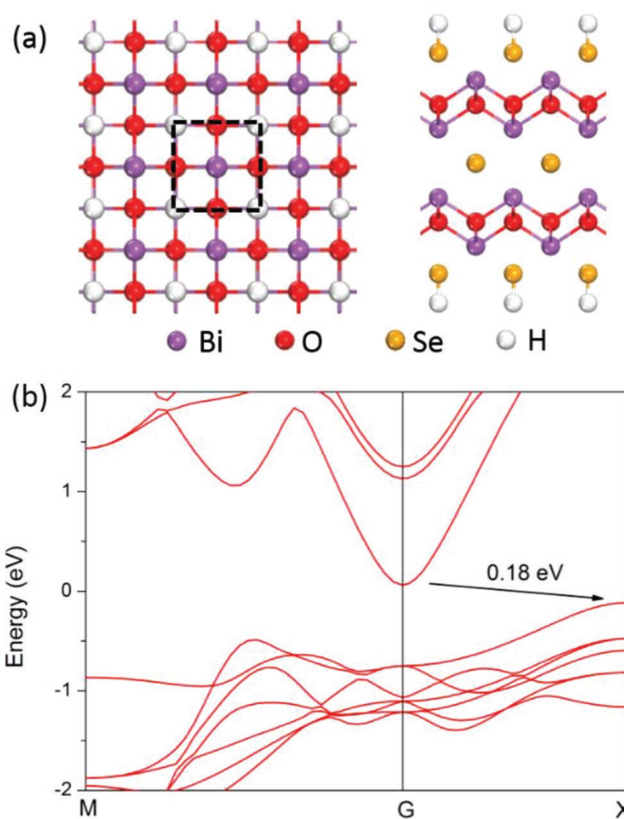

Figure 1. Lattice and electronic structure of BL Bi_2O_2Se. a) Top and side views of BL Bi_2O_2Se structure. b) Band structure of BL Bi_2O_2Se.

© 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

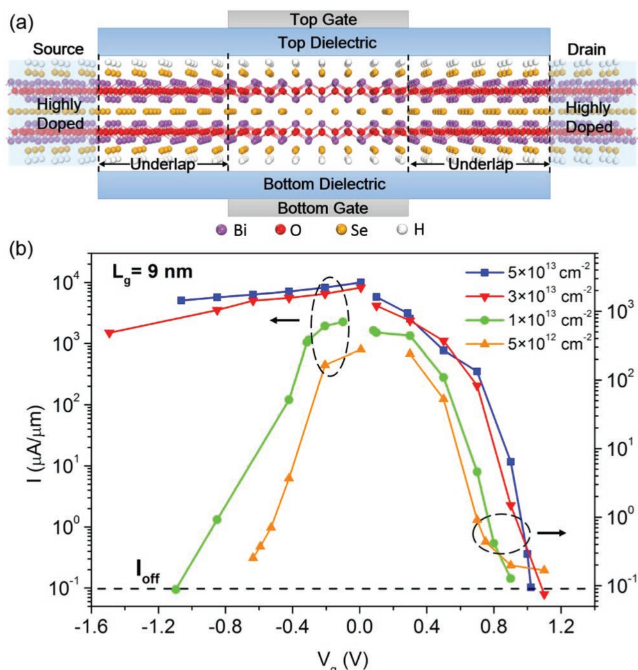

Figure 2. a) Schematic view of the DG BL Bi_2O_2Se MOSFET. b) Transfer characteristics for different source and drain doping concentration of electron (N_e) (left-hand axis) and hole (N_h) (right-hand axis) with L_g = 9 nm.

between the gate and the electrode are UL constitutions. Symmetric UL lengths (L_{UL}) of 0, 2, and 4 nm are considered. The equivalent oxide thicknesses (EOTs) of the SiO_2 dielectric is set to 0.41–0.56 nm, and the supply voltage (V_{dd}) of each device is 0.64–0.72 V (=V_b), which are adapted to the ITRS requirements for HP devices in different L_g. Off-state current I_{off} is fixed at 0.1 μA μm^{-1}, the OFF current for HP application requirement of ITRS. Only HP devices are considered, because I_{ds} is difficult to converge to the order of magnitude of 10^{-5} μA μm^{-1}, the low power (LP) goal of ITRS. I_{on} is evaluated at a specific supply gate voltage (V_g (on) = V_b + V_g (off)). The key figures of merit of the ballistic performance are benchmarked against the ITRS requirements for HP devices in **Tables 1** and **2**.

In order to ensure the most efficient carrier injection, it is critical to employ the optimal doping concentration on the checked BL Bi_2O_2Se MOSFETs. The doping concentration ranging from 5 × 10^{12} to 5 × 10^{13} cm^{-2} are considered.[5] The transfer characteristics of the 9 nm gate length BL Bi_2O_2Se n- and p-MOSFETs without UL at the bias of 0.72 V in four doping concentrations are plotted in Figure 2b.The optimized electron (hole) doping concentration of the BL Bi_2O_2Se n (p)-MOSFET is N_e = 1 × 10^{13} cm^{-2} (N_h = 5 × 10^{13} cm^{-2}) because the BL Bi_2O_2Se n (p)-MOSFET in this circumstance can not only reach the off-state of the HP requirement of ITRS in 2022 horizon but also possess the maximum I_{on} and the minimum subthreshold swing (SS) compared with other cases (Table S1, Supporting Information) simultaneously.

3.2. Current

In a logic switch, a high on-state current implies a high operating speed and is one of the key figures of merit of the device performance, especially for the HP servers.[54,55] The typical transfer characteristics of the n- and p-type sub 10 nm DG BL Bi_2O_2Se MOSFETs without UL at biases of V_b = 0.72, 0.69, 0.64, and 0.64 V with L_g = 9, 7, 5, and 3 nm, respectively, are shown in **Figure 3**. All p-MOSFETs have small enough source–drain leakage currents to fulfill the OFF state requirement

Table 1. Benchmark of the ballistic performance of the BL Bi_2O_2Se n-MOSFETS against the ITRS 2013 requirements for HP transistors of the next decades.

	L_g [nm]	L_{UL} [nm]	EOT [nm]	V_{dd} [V]	SS [mV dec^{-1}]	I_{on} [μA μm^{-1}]	I_{off} [μA μm^{-1}]	C_t [fF μm^{-1}]	τ [ps]	PDP [fJ μm^{-1}]
	9	0	0.54	0.72	111	1144	0.1	0.558	0.351	0.289
		2			102	1794	0.1	0.522	0.210	0.270
		4			112	–a)	–a)	0.486	–a)	–a)
ITRS 2022	8.8					1350	0.1	0.87	0.463	0.45
	7	0	0.49	0.69	117	–a)	–a)	0.383	–a)	–a)
		2			100	938	0.1	0.356	0.261	0.169
		4			118	1302	0.1	0.437	0.231	0.208
ITRS 2024	7.3					1170	0.1	0.77	0.451	0.36
	5	0	0.41	0.64	146	–a)	–a)	0.302	–a)	–a)
		2			105	–a)	–a)	0.323	–a)	–a)
		4			114	916	0.1	0.343	0.240	0.141
ITRS 2028	5.1					900	0.1	0.60	0.423	0.24
	3	0	0.41	0.64	322	–a)	–a)	0.253	–a)	–a)
		2			141	–a)	–a)	0.235	–a)	–a)
		4			134	–a)	–a)	0.213	–a)	–a)

a)ITRS I_{off} standard cannot be reached in our investigate gate voltage region. L_g: the gate length. EOT: the equivalent oxide thickness. SS: the subthreshold swing. V_{dd}: the supply voltage. I_{on}: the on-state current. I_{off}: the off-state current. C_t: the total capacitance. τ: the delay time. PDP: the power dissipation.

© 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

Table 2. Benchmark of the ballistic performance of the BL Bi_2O_2Se p-MOSFETS against the ITRS 2013 requirements for HP transistors of the next decades.

	L_g [nm]	L_{UL} [nm]	EOT [nm]	V_{dd} [V]	SS [mV dec^{-1}]	I_{on} [µA µm^{-1}]	I_{off} [µA µm^{-1}]	C_t [fF µm^{-1}]	τ [ps]	PDP [fJ µm^{-1}]
	9	0	0.54	0.72	86	779	0.1	0.729	0.675	0.378
		2			65	958	0.1	0.553	0.414	0.289
		3			84	1039	0.1	0.525	0.363	0.272
		4			73	631	0.1	0.420	0.486	0.218
ITRS 2022	8.8					1350	0.1	0.87	0.463	0.45
	7	0	0.49	0.69	102	729	0.1	0.599	0.567	0.285
		2			83	720	0.1	0.474	0.456	0.226
		4			65	477	0.1	0.345	0.414	0.164
ITRS 2024	7.3					1170	0.1	0.77	0.451	0.36
	5	0	0.41	0.64	181	275	0.1	0.467	1.077	0.190
		2			96	585	0.1	0.342	0.375	0.140
		4			60	540	0.1	0.276	0.327	0.113
ITRS 2028	5.1					900	0.1	0.60	0.423	0.24
	3	0	0.41	0.64	400	2	0.1	0.311	99.387	0.127
		2			320	18	0.1	0.272	9.984	0.111
		4			172	221	0.1	0.219	0.624	0.090

L_g: the gate length. EOT: the equivalent oxide thickness. SS: the subthreshold swing. V_{dd}: the supply voltage. I_{on}: the on-state current. I_{off}: the off-state current. C_t: the total capacitance. τ: the delay time. PDP: the power dissipation.

of HP device (0.1 µA µm^{-1}) and share the similar maximal current I_{max}.[8,54] However, the on current I_{on} is different from I_{max} because it is evaluated at a specific gate voltage window (V_g (on) = V_b + V_g (off)), where V_b is the bias voltage, V_g (on) and V_g (off) are the gate voltage of ON state and OFF state, respectively. I_{on} of these p-MOSFETs at L_g = 9, 7, 5, and 3 nm is 779, 729, 275, and 2 µA µm^{-1}, respectively, much lower than the corresponding ITRS HP required 1350, 1170, 900, and 900 µA µm^{-1}. All the checked n-MOSFETs could not reach the OFF state except for the 9 nm L_g device. I_{on} of BL Bi_2O_2Se n-MOSFET at L_g = 9 nm is 1144 µA µm^{-1}, fulfilling the 85% ITRS requirement (1350 µA µm^{-1}) for HP devices.

It is noteworthy that the n-MOSFET possesses a higher on-state current than that of the p-MOSFET at L_g = 9 nm. The reason lies in the smaller electron effective mass and the faster electron velocity of the n-MOSFET. The effective mass is proportional to the reciprocal of the curvature of the band dispersion spectrum. From the perspective of the band dispersion spectrum of Figure 1b, the electron effective mass is smaller than the hole one in BL Bi_2O_2Se ($m_e^* = 0.11\ m_0$ and, $m_h^* = 0.81\ m_0$, m_0 is the free-electron mass). Smaller effective mass increases the carrier velocity according to $v = \frac{1}{h}\frac{dE}{dk} = \frac{\hbar k}{m^*}$ and thus the current. It is also worth mentioning that larger effective mass can more

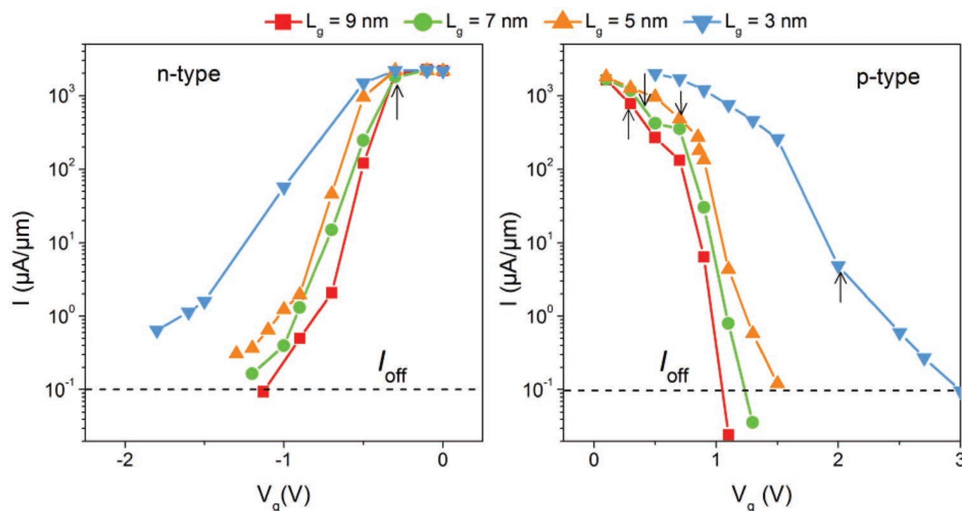

Figure 3. Transfer characteristics for the n- and p-type DG BL Bi_2O_2Se MOSFETs at different L_g. The black dash line represents I_{off} required by the ITRS 2013 for HP devices. The black arrow labels the position of I_{on} in different L_g.

© 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

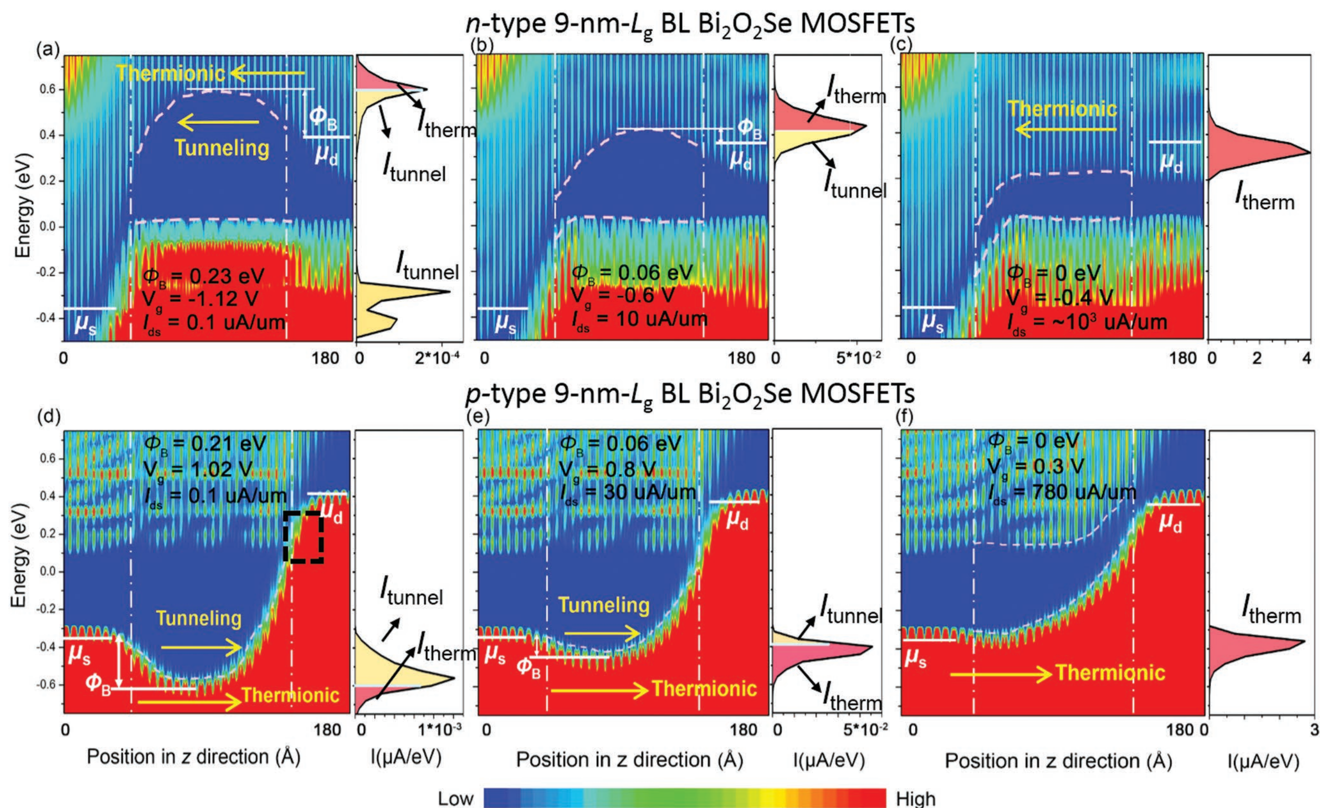

Figure 4. Position resolved local density of states (LDOS) and the spectrum current in the channel region for the n-type and p-type 9 nm L_g DG BL Bi_2O_2Se MOSFETs under V_b = 0.72 V. a–c) 9 nm L_g n-MOSFET at V_g = –1.12, –0.6, and –0.4 V for OFF state, the intermediate state and ON state, respectively. e–g) 9 nm L_g p-MOSFET at V_g = 1.02, 0.8, and 0.3 V for OFF state, the intermediate state and ON state, respectively. μ_s and μ_d are the electrochemical potential of the source and drain, respectively. Φ_B is the effective barrier height. The white dash dot lines are the edges of gate. The yellow dash arrows represent the thermionic and tunneling electron transports.

easily block the tunneling leakage because I_{tunnel} decreases exponentially with the effective mass, i.e., $I_{tunnel} \propto e^{-l\sqrt{m^*\Phi_B}}$, where l and Φ_B are the width and the height of the barrier respectively. As a result, the BL Bi_2O_2Se p-MOSFETs are much easier to reach OFF state than the n-MOSFETs.

To unveil the gate modulation and the current change mechanism, the position resolved local density of states (LDOS) and the spectrum current of the 9 nm L_g n-MOSFET and the 9 nm L_g p-MOSFET at different gate voltages (V_g) are shown in **Figure 4**. I_{ds} is composed by tunneling current (I_{tunnel}) and thermionic current (I_{therm}). I_{tunnel} and I_{therm} are separated by the top of Φ_B. In the OFF state (I_{ds} = 0.1 μA $μm^{-1}$) of the 9 nm L_g n-MOSFET (Figure 4a) with V_g = –1.12 V and Φ_B = 0.23 eV, the conduction band minimum (CBM) and the valence band maximum (VBM) of the channel are lifted by V_g. I_{tunnel} at low energy level stems from the tunneling from the VB to the CB within the left electrode (Figure 4a). In the intermediate state (I_{ds} = 10 μA $μm^{-1}$) of the 9 nm L_g n-MOSFET with V_g = –0.6 V (Figure 4b), the upward degree of the CBM of the channel is alleviated and Φ_B decreases to 0.06 eV. I_{tunnel} and I_{therm} sharply increase by two orders of magnitude. In the ON state (I_{ds} = ≈1000 μA $μm^{-1}$) of the 9 nm L_g n-MOSFET (Figure 4c), the supply V_g = –0.4 V releases the upward degree of the CBM of the channel and diminishes Φ_B. I_{therm} dominates the total current. The VBM of the channel in the intermediate state and ON state is not lifted upward. I_{tunnel} at the VB is much smaller than I_{tunnel} and I_{therm} at the CB.

The gate modulation of the 9 nm L_g p-MOSFET (Figure 4d–f) is similar to that of the 9 nm L_g n-MOSFET. From the OFF state (Figure 4d) to the intermediate state (Figure 4e) and to the ON state (Figure 4f), the downward degree of the VBM of the channel is gradually alleviated, Φ_B decreases from 0.21 to 0 eV, and I_{therm} dominates the total current. Even if Φ_B is vanished, I_{on} can only reach few hundreds of μA $μm^{-1}$ because of the heavier hole effective mass. In spite of the fact that the CB connects to the VB at the right edge of the gate, no current component is observed at this energy range (labeled a black dash square in Figure 4d). This is because the local and discontinuous states in the VB impede electrons moving from the LDOS in Figure 4d–f.

To get a high on-state current, UL as an improvement method can extend the effective channel length, impede the short channel effects and thus effectively boost the device performance. On the other hand, the gate controlling capacity to the uncovered channel region is weaker than the covered one, and too long UL will degrade the device performance. Therefore, the length of UL has to be optimized.[54] The transfer characteristics of the BL Bi_2O_2Se n- and p- MOSFETs with different L_{UL} are compared in Figures S2 and S3 in the Supporting Information respectively. We benchmark I_{on} versus L_g for the HP DG BL

© 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

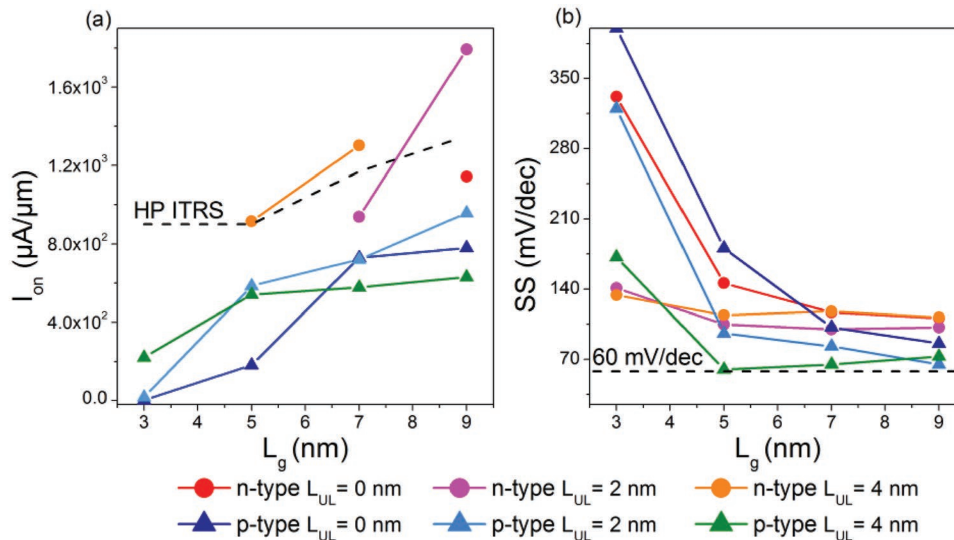

Figure 5. a) HP-I_{on} and b) SS versus L_g for the n- and p-type DG BL Bi_2O_2Se MOSFETs at different L_{UL} as indicated in the legend.

Bi_2O_2Se MOSFETs against the ITRS standards in **Figure 5**a. L_{UL} = 2 nm is the optimal length for the 9 nm L_g n-MOSFET because I_{on} is maximized with a value of 1794 μA μm^{-1} (Table 1), which exceeds the ITRS HP goal (1350 μA μm^{-1}), while L_{UL} = 4 nm is so long that the leakage current could not meet the HP OFF state requirement. L_{UL} = 4 nm is the optimal length for both the 7 and 5 nm L_g n-MOSFETs because I_{on} is maximized with values of 1302 and 916 μA μm^{-1} and exceeds the ITRS required 1170 and 900 μA μm^{-1} for HP applications, respectively. Hence, the n-MOSFETs with proper UL could extend the Moore's law down to 5 nm. The 3 nm L_g n-MOSFETs with different L_{UL} are still vulnerable to the short channel effect and the ITRS required OFF state could not be fulfilled.

L_{UL} = 3 nm is the optimal length for the 9 nm L_g p-MOSFET because I_{on} is maximized with the value of 1039 μA μm^{-1}, which reaches 77% of the ITRS HP requirement, while L_{UL} = 4 is so long that I_{on} is decreased to 49% of the ITRS HP requirement. The 7 nm L_g p-MOSFETs with different L_{UL} could not produce higher I_{on} (720 μA μm^{-1} for L_{UL} = 2 nm, 577 μA μm^{-1} for L_{UL} = 4 nm) compared with the 7 nm L_g p-MOSFET without UL (729 μA μm^{-1}). I_{on} of the 5 nm L_g p-MOSFETs doubles to 584 and 570 μA μm^{-1}, respectively, when L_{UL} = 2 and 4 nm are adopted. As L_{UL} extends from 0 to 2 and to 4 nm, I_{on} of the 3 nm L_g p-MOSFET increases dramatically from 2 to 18 and to 221 μA μm^{-1}, respectively. However, even if in some cases the p-MOSFETs with UL induces higher I_{on}, none of these I_{on} could meet the ITRS goals for HP applications.

3.3. Subthreshold Swing

Apart from I_{on}, SS is also one of the key figures of merit for device performance evaluation. SS is expressed as $SS = \frac{\partial V_g}{\partial \lg I_{ds}}$, which means the incremental gate voltage applied to change the current by one decade and indicates the device gate controlling ability.[8] The smaller SS, the better gate controlling. The SS values versus different L_g of DG BL Bi_2O_2Se n- and p-MOSFETs are plotted in Figure 5b. As L_g scales down, SS sharply increases with values of 111, 117, 146, and 322 mV dec^{-1} (86, 105, 181, and 400 mV dec^{-1}) for Bi_2O_2Se n (p)-MOSFETs with L_g = 9, 7, 5, and 3 nm, respectively.

The UL helps reduce SS and improve the gate electrostatics. The effect of UL on the SS of $L_g \leq 5$ nm n-MOSFETs is remarkable. SS of the 5 nm (3 nm) L_g n-MOSFET with L_{UL} = 2 nm is reduced by 28% (58%). However, with the increasing L_g, the improvement on SS by UL is less apparent. Despite of the improvement of UL on the n-MOSFETs, the SS value still surpasses 100 mV dec^{-1} and far exceeds the ideal 60 mV dec^{-1}.

The 9 nm L_g p-MOSFETs with UL has smaller SS value and better gate electrostatics in the subthreshold region. This difference stems from the heavier hole effective mass ($m_h^* : m_e^* = 8:1$), which prefers to suppress the source–drain leakage current and to form smaller SS. SS of the 7, 5, and 3 nm L_g p-MOSFETs with L_{UL} = 4 nm is reduced by 36%, 67%, and 57%, respectively. Notably, the SS of the 7 nm L_g p-MOSFET in L_{UL} = 4 nm is 65 mV dec^{-1} and the 5 nm L_g p-MOSFET in L_{UL} = 4 nm is 60 mV dec^{-1}, near to the limit of the ideal thermionic transistors (60 mV dec^{-1}).[2,8,56,57]

Above threshold region, we extract transconductance (g_m) to evaluate the gate control (Figure S1, Supporting Information). All n-MOSFETs have larger g_m (2.6–7.0 mS μm^{-1}) than the p-MOSFETs (1.8–3.4 mS μm^{-1}), which indicates a better superthreshold gate control of the n-MOSFETs.

3.4. Intrinsic Delay Time and Power Consumption

The capacitance (C_t) and the intrinsic delay time (τ) are another two crucial factors of logic switch. C_t is defined as the total capacitance composed by gate capacitance (C_g) and fringing capacitance (C_f). C_g is calculated by $Cg = \frac{\partial Qch}{\partial Vg}$, where Q_{ch} is the total charge of the central region. C_f is the twice of C_g according to the ITRS standards. The C_t of the BL Bi_2O_2Se n- and p-MOSFETs in different L_g is 0.213–0.558 and 0.219–0.729 fF μm^{-1}, respectively. The switching speed is directly characterized by τ, which is calculated by the formula: $\tau = \frac{CtVdd}{Ion}$, where V_{dd} is the

© 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

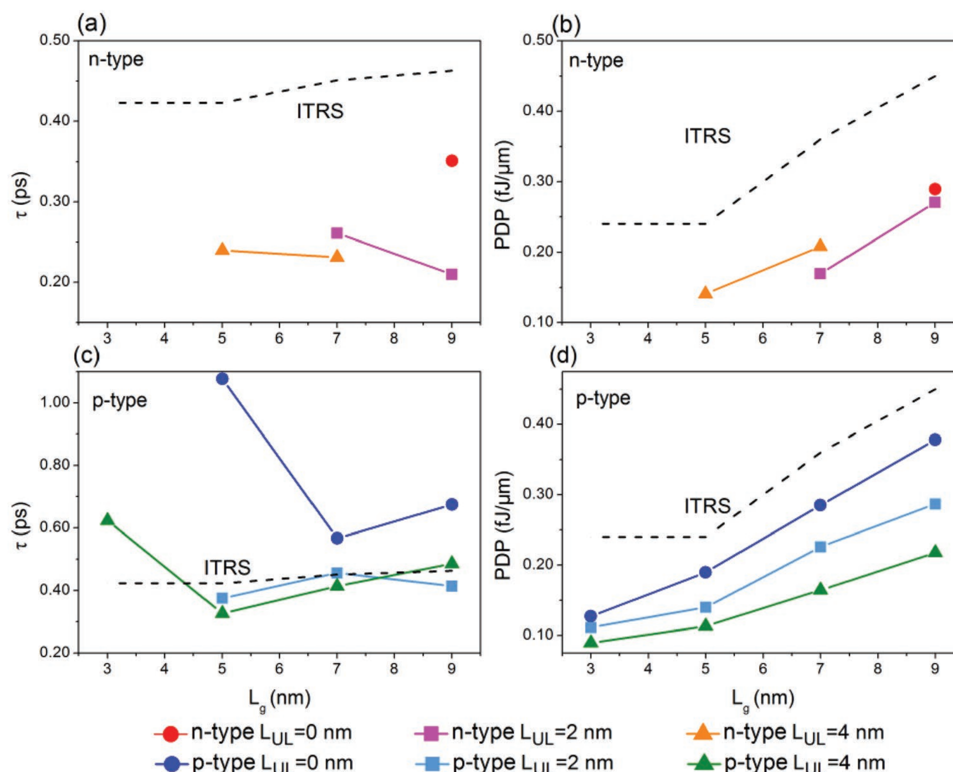

Figure 6. a) Intrinsic delay time and b) the power dissipation as functions of the gate length in the n-type DG BL Bi_2O_2Se MOSFETs with different L_{UL}. c) Same as (a) but for the p-type DG BL Bi_2O_2Se MOSFETs. d) Same as (b) but for the p-type DG BL Bi_2O_2Se MOSFETs. The black dash lines are the ITRS HP requirements for delay time and PDP.

supply voltage. If I_{on} is effectively defined (Tables 1 and 2), τ of a device can be figured out. The calculated τ (0.210–0.351 ps) of all the BL Bi_2O_2Se n-MOSFETs can meet the ITRS requirement for HP devices in next decade horizons. Only τ of the 5 nm L_g with $L_{UL} = 0$ and 2 nm, 7 nm L_g with $L_{UL} = 4$ nm, and 9 nm L_g with $L_{UL} = 2$ nm p-MOSFETs can meet the ITRS HP requirements. UL could effectively shorten τ, as shown in **Figure 6**a,c. For example, τ of the 5 nm L_g p-MOSFETs with $L_{UL} = 0$, 2, and 4 nm is 0.599, 0.474, and 0.325 ps, respectively. As a result of small τ, BL Bi_2O_2Se MOSFETs with UL will be a logic transistor with a fast switching speed.

Power consumption is an important indicator concerning the switching energy. PDP = $V_{dd}I_{on}\tau$. If I_{on} can be effectively defined, PDP of a device can be calculated. From Figure 6b,d, PDP of the BL Bi_2O_2Se p-MOSFETs monotonically decreases with the decreasing L_g. The longer L_{UL}, the smaller PDP. All the calculated PDP (0.090–0.378 fJ μm^{-1}) of the sub 10 nm L_g BL Bi_2O_2Se n- and p-MOSFETs could meet the ITRS HP requirement. For example, the largest PDP is 0.378 fJ μm^{-1} for the case of 9 nm L_g BL Bi_2O_2Se p-MOSFET, much lower than the minimum value of the ITRS HP required 0.45 fJ μm^{-1}.

4. Discussion

The heavily doped BL Bi_2O_2Se is employed as electrodes in our calculated BL Bi_2O_2Se MOSFETs, and there is no Schottky barrier in the interface between the electrode and the channel. However, there is no reliable substitutional method to dope 2D materials directly in the experiment.[5] Experimentally, metal electrode is often chosen to directly contact with 2D semiconductors and inject carriers to 2D semiconducting channel. Such a configuration often leads to a formation of Schottky barrier at the metal-semiconductor interface, and the corresponding FET is called Schottky barrier FET (SBFET). However, Schottky barrier could be eliminated by formation of Ohmic contacts with proper metal electrodes. In this case, the device performance of the SBFET may approach that of the corresponding MOSFET. For instance, when graphene as an electrode is employed in the ML BP SBFET, I_{on} of this device reaches ≈90% of that of the BP MOSFET because graphene forms an Ohmic contact with BP.[28,54] The fabricated long-channeled BL Bi_2O_2Se FET using Au/Pd as the electrode forms Ohmic contacts, which is in great accordance with our calculation.[58] Besides, Au, Pd, Pt, Ti, and Sc could also lead Ohmic contacts with BL Bi_2O_2Se based on ab initio quantum transporting calculations.[58] With these Ohmic contacts, the performance of the BL Bi_2O_2Se SBFET is expected to approach the MOSFET limit.

Next, we compare the BL Bi_2O_2Se MOSFETs with the most commonly studied BP and MoS_2 counterparts. ML BP MOSFETs are predicted to show on-currents that could meet the ITRS HP/LP goals and extend Moore's law down to 2 nm on the basis of the previous calculations.[54] This device performance is superior to that of the BL Bi_2O_2Se MOSFETs. However, the BL Bi_2O_2Se has more excellent air stability than BP. Since the stability is a precondition for large-scale production,

 © 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

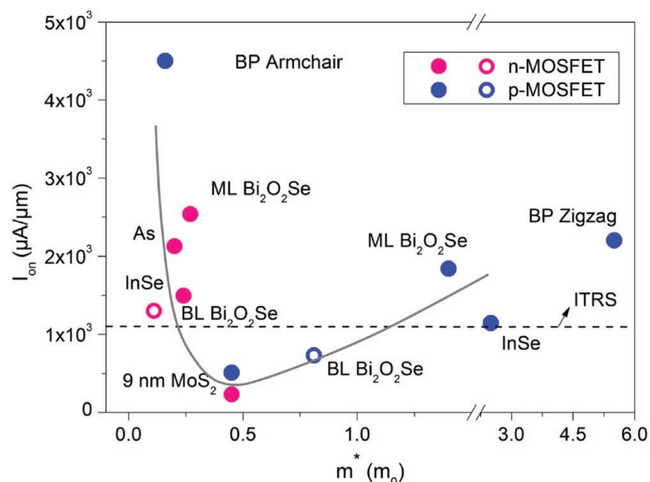

Figure 7. On-state current of the n- and p-MOSFETs at $L_g = 7$ nm versus the effective mass of 2D channel materials. All data is calculated by ab initio quantum transport simulations.[5,54,60,61] The dash line is the ITRS HP requirement of the 2013 edition. The solid line is guidance to the eyes.

BL Bi_2O_2Se is more feasible to be a candidate of the next-generation channel material. Compared with the air-stable ML MoS_2 MOSFET, BL Bi_2O_2Se MOSFET shows an advantage in the on-current. The optimal I_{on} of the ML MoS_2 n-MOSFET with L_{UL} only fulfill 50% of the ITRS HP goal,[59] but the optimal I_{on} of the BL Bi_2O_2Se n-MOSFET with L_{UL} exceeds the HP requirement based on our calculations given $L_g = 5$ nm.

To get the dependence of I_{on} on different effective masses, we plot the function of I_{on} of the n- and p-MOSFETs versus the effective mass of different 2D channel materials at $L_g = 7$ nm in **Figure 7** (the ML MoS_2 MOSFETs are at $L_g = 9$ nm), on the basis of previous simulations.[54,55,60,61] Along with m* increasing, I_{on} has a decreasing tendency when $m^* \le 0.45\ m_0$ for n-MOSFETs and an increasing tendency when $m^* \ge 0.45\ m_0$ for p-MOSFETs. This is because a contradiction exists between small m*and large I_{on}. Small m* speeds up carrier velocity and thus large I_{on}. However, small m* goes against to sufficient density of states (DOS) near the VBM and CBM ($\mathrm{DOS} = \frac{g_s g_v}{2\pi\hbar^2}\sqrt{m_x^* m_y^*}$, where g_s and g_v stand for the spin and valley degeneracies, respectively, and x and y represent for the transverse and transport directions, respectively). Insufficient DOS could not guarantee sufficient current drive.[61] It's noteworthy that the anisotropic ML armchair-directed BP p-MOSFET, whose $m_x^* = 0.16\ m_0$ and $m_y^* = 5.40\ m_0$ for the holes, possesses small m*, adequate DOS simultaneously, and thus achieves extremely high I_{on} ((4500 μA μm^{-1}).[28] In the cases of ML MoS_2, ML/BL Bi_2O_2Se, InSe, and zigzag-directed BP p-MOSFETs, the large DOS near the VBM produces benefits to I_{on}. For other cases of ML MoS_2, ML/BL Bi_2O_2Se, InSe, and arsenene n-MOSFETs, the high carrier velocity gives advantage on their I_{on}. It's intriguing that BL Bi_2O_2Se has smaller m_e^* and higher carrier velocity but its MOSFET has a comparably lower I_{on} compared with tendency curve of the ML FETs.

As the semiconductor channel thickness increases, the carrier of channel increases, but the control ability of the gate on the channel is weakened. Generally, the device performance is degraded with the increasing layer number, reflecting the dominative role of the reduced gate control ability. For example, as the channel thickness increases from 1.3 to 12 nm, SS of the 1 nm L_g MoS_2 FET extremely raises up to 170 mV dec^{-1}, and the device could not be turned off when the thickness of MoS_2 is increased to ≈31 nm.[1] But for monolayer and bilayer 2D materials, these two effects are compelling with each other. The ML and BL BP FETs exhibit similar gate electrostatics abilities (SS = 62–66 mV dec^{-1}) and I_{on} (a few thousand microampere per micrometer).[62] By contrast, bilayer MoS_2 FET (SS = 109 mV dec^{-1} and $I_{on}/I_{off} = 10^4$) shows a weaker gate control and less on/off ratio compared with monolayer MoS_2 (SS = 84 mV dec^{-1} and $I_{on}/I_{off} = 10^5$) based on tight-binding models.[63]

There are two causes for the poorer device performance for the BL Bi_2O_2Se FETs than the ML counterpart. One is the reduced gate electrostatics, and the other is the much smaller bandgap of ≈0.18 eV in BL Bi_2O_2Se (compared with a bandgap of ≈1.14 eV in ML Bi_2O_2Se). The much smaller bandgap greatly increases the leakage current, making the off state difficult to access in the BL Bi_2O_2Se FETs. As the layer number continuously increases to 11, the bandgap continuously decreases nearly to 0 eV in terms of the previous calculation.[32] Hence the leak current issue becomes more serious in addition to the reduced gate electrostatics. Thus, the device performance of the sub 10 nm few layer Bi_2O_2Se MOSFETs is expected to degrade.

The light effective mass and sizeable bandgap might be applicable to other bismuth oxychalcogenides, such as Bi_2O_2S and Bi_2O_2Te. The band structures of Bi_2O_2S and Bi_2O_2Te are shown in Figure S5 in the Supporting Information. The bandgaps of the ML and BL Bi_2O_2S are evaluated as ≈1.77 and 0.83 eV, respectively, larger than the BL Bi_2O_2Se. ML (BL) Bi_2O_2S has a small electron effective mass with the value of 0.15 m_0 (0.13 m_0). The bandgaps of the ML and BL Bi_2O_2Te are evaluated as ≈0.20 and 0 eV, respectively. The electron effective mass of ML Bi_2O_2Te is also small (0.09 m_0). Combining the sizeable bandgap with the quite light effective mass, ML/BL Bi_2O_2S might show performance even better than BL Bi_2O_2Se.

5. Conclusion

Inspired by the emerging air-stable 2D Bi_2O_2Se FET with high performance, the device performance of sub 10 nm L_g DG BL Bi_2O_2Se MOSFETs has been studied using ab initio quantum transport simulations for the first time. All the checked BL Bi_2O_2Se p-MOSFETs have smaller on-state current with respect to the n-MOSFETs due to the heavier hole effective mass. In absence of underlap structure, I_{on} of the BL Bi_2O_2Se n-MOSFETs can not meet ITRS requirement, and the highest I_{on} can only reach ≈80% ITRS HP requirement at $L_g = 9$ nm. However, with the resort of underlap, the BL Bi_2O_2Se n-MOSFETs can fulfill the HP requirements of ITRS 2013 edition until the gate length is scaled down to 5 nm. Hence, BL Bi_2O_2Se is a potential channel material for sub 10 nm FETs.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

 © 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

Acknowledgements

This work was supported by the National Key Research and Development Program of China (No. 2017YFA206303), the National Natural Science Foundation of China (Nos. 11674005 and 5173100), the National Materials Genome Project of China (No. 2016YFB0700600) and supported by the High Performance Computing Platform of Peking University, China. L.X. was supported by the Key Research and Development Program of Ningxia in China (No. 2018BEE03023).

Conflict of Interest

The authors declare no conflict of interest.

Keywords

ab initio quantum transport calculations, bilayer Bi_2O_2Se, high performance limit, sub 10 nm transistors

Received: October 13, 2018
Revised: December 27, 2018
Published online: February 4, 2019

[1] S. B. Desai, S. R. Madhvapathy, A. B. Sachid, J. P. Llinas, Q. Wang, G. H. Ahn, G. Pitner, M. J. Kim, J. Bokor, C. Hu, H. S. P. Wong, A. Javey, *Science* **2016**, *354*, 99.
[2] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee, L. Colombo, *Nat. Nanotechnol.* **2014**, *9*, 768.
[3] C. Qiu, Z. Zhang, M. Xiao, Y. Yang, D. Zhong, L.-M. Peng, *Science* **2017**, *355*, 271.
[4] Z. Ni, M. Ye, J. Ma, Y. Wang, R. Quhe, J. Zheng, L. Dai, D. Yu, J. Shi, J. Yang, S. Watanabe, J. Lu, *Adv. Electron. Mater.* **2016**, *2*, 1600191.
[5] Y. Wang, P. Huang, M. Ye, R. Quhe, Y. Pan, H. Zhang, H. Zhong, J. Shi, J. Lu, *Chem. Mater.* **2017**, *29*, 2191.
[6] F. Gao, H. Yang, P. Hu, *Small Methods* **2018**, *2*, 1700384.
[7] F. Schwierz, *Nat. Nanotechnol.* **2010**, *5*, 487.
[8] F. Schwierz, J. Pezoldt, R. Granzner, *Nanoscale* **2015**, *7*, 8261.
[9] J. Yang, R. Quhe, S. Feng, Q. Zhang, M. Lei, J. Lu, *Phys. Chem. Chem. Phys.* **2017**, *19*, 23982.
[10] A. F. Morpurgo, *Nat. Phys.* **2015**, *11*, 625.
[11] J. Kang, W. Liu, D. Sarkar, D. Jena, K. Banerjee, *Phys. Rev. X* **2014**, *4*, 031005.
[12] Y. Wang, R. X. Yang, R. Quhe, H. Zhong, L. Cong, M. Ye, Z. Ni, Z. Song, J. Yang, J. Shi, J. Li, J. Lu, *Nanoscale* **2016**, *8*, 1179.
[13] R. Quhe, Y. Wang, M. Ye, Q. Zhang, J. Yang, P. Lu, M. Lei, J. Lu, *Nanoscale* **2017**, *9*, 14047.
[14] Q. Li, J. Yang, R. Quhe, Q. Zhang, L. Xu, Y. Pan, M. Lei, J. Lu, *Carbon* **2018**, *135*, 125.
[15] Y. Cai, G. Zhang, Y.-W. Zhang, *J. Phys. Chem. C* **2015**, *119*, 13929.
[16] H. Liu, A. T. Neal, Z. Zhu, Z. Luo, X. Xu, D. Tománek, P. D. Ye, *ACS Nano* **2014**, *8*, 4033.
[17] S. Fukuoka, T. Taen, T. Osada, *J. Phys. Soc. Jpn.* **2015**, *84*, 121004.
[18] S. Das, H.-Y. Chen, A. V. Penumatcha, J. Appenzeller, *Nano Lett.* **2013**, *13*, 100.
[19] D. Voiry, R. Fullon, J. Yang, C. de Carvalho Castro e Silva, R. Kappera, I. Bozkurt, D. Kaplan, M. J. Lagos, P. E. Batson, G. Gupta, A. D. Mohite, L. Dong, D. Er, V. B. Shenoy, T. Asefa, M. Chhowalla, *Nat. Mater.* **2016**, *15*, 1003.
[20] X. Chen, H. Yang, G. Liu, F. Gao, M. Dai, Y. Hu, H. Chen, W. Cao, P. Hu, W. Hu, *Adv. Funct. Mater.* **2018**, *28*, 1705153.
[21] K. Xu, D. Chen, F. Yang, Z. Wang, L. Yin, F. Wang, R. Cheng, K. Liu, J. Xiong, Q. Liu, J. He, *Nano Lett.* **2017**, *17*, 1065.
[22] A. Carvalho, M. Wang, X. Zhu, A. S. Rodin, H. Su, A. H. Castro Neto, *Nat. Rev. Mater.* **2016**, *1*, 16061.
[23] K. Watanabe, T. Taniguchi, H. Kanda, *Nat. Mater.* **2004**, *3*, 404.
[24] M. Dai, H. Chen, R. Feng, W. Feng, Y. Hu, H. Yang, G. Liu, X. Chen, J. Zhang, C.-Y. Xu, P. Hu, *ACS Nano* **2018**, *12*, 8739.
[25] W. Feng, W. Zheng, W. Cao, P. Hu, *Adv. Mater.* **2014**, *26*, 6587.
[26] P. Hu, L. Wang, M. Yoon, J. Zhang, W. Feng, X. Wang, Z. Wen, J. C. Idrobo, Y. Miyamoto, D. B. Geohegan, K. Xiao, *Nano Lett.* **2013**, *13*, 1649.
[27] J. D. Wood, S. A. Wells, D. Jariwala, K.-S. Chen, E. Cho, V. K. Sangwan, X. Liu, L. J. Lauhon, T. J. Marks, M. C. Hersam, *Nano Lett.* **2014**, *14*, 6964.
[28] R. Quhe, X. Peng, Y. Pan, M. Ye, Y. Wang, H. Zhang, S. Feng, Q. Zhang, J. Shi, J. Yang, D. Yu, M. Lei, J. Lu, *ACS Appl. Mater. Interfaces* **2017**, *9*, 3959.
[29] L. Kou, C. Chen, S. C. Smith, *J. Phys. Chem. Lett.* **2015**, *6*, 2794.
[30] J. Wu, Y. Liu, Z. Tan, C. Tan, J. Yin, T. Li, T. Tu, H. Peng, *Adv. Mater.* **2017**, *29*, 1704060.
[31] J. Wu, C. Tan, Z. Tan, Y. Liu, J. Yin, W. Dang, M. Wang, H. Peng, *Nano Lett.* **2017**, *17*, 3021.
[32] J. Wu, H. Yuan, M. Meng, C. Chen, Y. Sun, Z. Chen, W. Dang, C. Tan, Y. Liu, J. Yin, Y. Zhou, S. Huang, H. Q. Xu, Y. Cui, H. Y. Hwang, Z. Liu, Y. Chen, B. Yan, H. Peng, *Nat. Nanotechnol.* **2017**, *12*, 530.
[33] T. Low, A. S. Rodin, A. Carvalho, Y. Jiang, H. Wang, F. Xia, A. H. Castro Neto, *Phys. Rev. B* **2014**, *90*, 075434.
[34] S.-L. Li, K. Tsukagoshi, E. Orgiu, P. Samori, *Chem. Soc. Rev.* **2016**, *45*, 118.
[35] M. Wu, X. C. Zeng, *Nano Lett.* **2017**, *17*, 6309.
[36] A. K. Geim, K. S. Novoselov, *Nat. Mater.* **2007**, *6*, 183.
[37] P. Hu, Z. Wen, L. Wang, P. Tan, K. Xiao, *ACS Nano* **2012**, *6*, 5988.
[38] International Technology Roadmap for Semiconductors (ITRS), http://www.itrs2.net (accessed: April 2014).
[39] M. Brandbyge, J.-L. Mozos, P. Ordejon, J. Taylor, K. Stokbro, *Phys. Rev. B* **2001**, *65*, 165401.
[40] M. S. José, A. Emilio, D. G. Julian, G. Alberto, J. Javier, O. Pablo, S.-P. Daniel, *J. Phys.: Condens. Matter* **2002**, *14*, 2745.
[41] Y. Pan, Y. Wang, L. Wang, H. Zhong, R. Quhe, Z. Ni, M. Ye, W.-N. Mei, J. Shi, W. Guo, J. Yang, J. Lu, *Nanoscale* **2015**, *7*, 2116.
[42] S. Datta, *Quantum Transport: Atom to Transistor*, Cambridge University Press, England **2005**.
[43] S. Datta, *Electronic Transport in Mesoscopic System*, Cambridge University Press, England **1995**.
[44] F. Pan, R. Quhe, Q. Ge, J. Zheng, Z. Ni, Y. Wang, Z. Gao, L. Wang, J. Lu, *Phys. E* **2014**, *56*, 43.
[45] J. P. Perdew, K. Burke, M. Ernzerhof, *Phys. Rev. Lett.* **1996**, *77*, 3865.
[46] R. Quhe, R. Fei, Q. Liu, J. Zheng, H. Li, C. Xu, Z. Ni, Y. Wang, D. Yu, Z. Gao, J. Lu, *Sci. Rep.* **2012**, *2*, 853.
[47] S. Das, W. Zhang, M. Demarteau, A. Hoffmann, M. Dubey, A. Roelofs, *Nano Lett.* **2014**, *14*, 5733.
[48] Y. Liang, L. Yang, *Phys. Rev. Lett.* **2015**, *114*, 063001.
[49] S. Liu, J. Li, B. Shi, X. Zhang, Y. Pan, M. Ye, R. Quhe, Y. Wang, H. Zhang, J. Yan, L. Xu, Y. Guo, F. Pan, J. Lu, *J. Mater. Chem. C* **2018**, *6*, 5651.
[50] Y. Zhang, T.-R. Chang, B. Zhou, Y.-T. Cui, H. Yan, Z. Liu, F. Schmitt, J. Lee, R. Moore, Y. Chen, H. Lin, H.-T. Jeng, S.-K. Mo, Z. Hussain, A. Bansil, Z.-X. Shen, *Nat. Nanotechnol.* **2013**, *9*, 111.
[51] Y. Pan, Y. Wang, M. Ye, R. Quhe, H. Zhong, Z. Song, X. Peng, D. Yu, J. Yang, J. Shi, J. Lu, *Chem. Mater.* **2016**, *28*, 2100.
[52] Y. Pan, Y. Dan, Y. Wang, M. Ye, H. Zhang, R. Quhe, X. Zhang, J. Li, W. Guo, L. Yang, J. Lu, *ACS Appl. Mater. Interfaces* **2017**, *9*, 12694.

© 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

[53] X. Zhang, Y. Pan, M. Ye, R. Quhe, Y. Wang, Y. Guo, H. Zhang, Y. Dan, Z. Song, J. Li, J. Yang, W. Guo, J. Lu, *Nano Res.* **2018**, *11*, 707.
[54] R. Quhe, Q. Li, Q. Zhang, Y. Wang, H. Zhang, J. Li, X. Zhang, D. Chen, K. Liu, Y. Ye, L. Dai, F. Pan, M. Lei, J. Lu, *Phys. Rev. A* **2018**, *10*, 024022.
[55] X. Sun, Z. Song, S. Liu, Y. Wang, Y. Li, W. Wang, J. Lu, *ACS Appl. Mater. Interfaces* **2018**, *10*, 22363.
[56] F. Liu, Y. Wang, X. Liu, J. Wang, H. Guo, *IEEE. Trans. Electron Devices* **2014**, *61*, 3871.
[57] Y. Taur, T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, England **2001**.
[58] L. Xu, S. Liu, J. Yang, B. Shi, Y. Pan, X. Zhang, H. Li, J. Yan, J. Li, L. Xu, J. Yang, J. Lu, unpublished, **2018**.
[59] H. Zhang, J. Lu, unpublished, **2018**.
[60] R. Quhe, J. Liu, J. Wu, J. Yang, Y. Wang, Q. Li, J. Yang, H. Peng, M. Lei, J. Lu, *Nanoscale* **2019**, *11*, 532.
[61] Y. Wang, R. Fei, R. Quhe, J. Li, H. Zhang, X. Zhang, B. Shi, L. Xiao, Z. Song, J. Yang, J. Shi, F. Pan, J. Lu, *ACS Appl. Mater. Interfaces* **2018**, *10*, 23344.
[62] D. Yin, G. Han, Y. Yoon, *IEEE. Electron Device Lett.* **2015**, *36*, 978.
[63] V. Mishra, S. Smith, L. Liu, F. Zahid, Y. Zhu, H. Guo, S. Salahuddin, *IEEE. Trans. Electron Devices* **2015**, *62*, 2457.

© 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim